A Light Tolerant Neural Recording IC for Near-Infrared-Powered Free Floating Motes

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Abstract

A key challenge for near-infrared (NIR) powered neural recording ICs is to maintain robust operation in the presence of parasitic short circuit current from junction diodes when exposed to light. This is especially so when intentional currents are kept small to reduce power consumption. We present a neural recording IC that is tolerant up to 300 µW/mm² light exposure (above tissue limit) and consumes 0.57 µW at 38°C, making it lowest power among standalone motes while incorporating on-chip feature extraction and individual gain control.

Introduction

Power transmission and communication are the key challenge for ultra-small (< 0.5mm) wireless neural recording motes and, among several approaches (RF, ultra-sound [1,2]), NIR using an integrated PV and LED is unique in its ability to scale linearly to very small sizes (< 100µm) [3,4]. Minimum size is critical to achieving dense recording arrays and minimum scattering and requires that radiated light power is maximized while chip power and currents are minimized. This leaves the circuits particularly susceptible to light-induced parasitic currents (Fig. 2). In conventional chips, light is blocked with an encapsulant. However, a partly transparent encapsulation that exposes the PV and LED while blocking light for sensitive circuits is infeasible at sub-mm scales leaving the solution to light tolerant circuit design. To our knowledge, this work is the first attempt to address this challenge.

The proposed IC achieves robust operation past the tissue limit NIR (150 µW/mm²) while a baseline implementation fails at 8µW/mm². The chip maintains sub-µW power while incorporating advanced functionality, including on chip feature extraction and gain control. The proposed work was tested with neural signals from a Long Evans rat and demonstrated high fidelity monkey finger motion decoding.

The envisioned system architecture is described in [4] and consists of a large number of free-floating motes on top of the brain that use the proposed optical mote can fully function under 300µW/mm² of light exposure (above tissue limit). The proposed IC was fabricated in 180nm CMOS (Fig. 11). In a fully wireless optical setup with an NIR laser for power transfer and downlink and SPAD detector for uplink reception (Fig. 10) the IC can achieve 68 dB peak gain, [380, 1060] Hz bandwidth, > 67dB of CMRR and PSRR and, IR of 6.2µVs with 150µW/mm² of incident 850nm LED light at 38°C in measurement which is nearly unchanged from that measured without light (Fig. 5, table). The graph in Fig. 5 plots measured gain across light level for a baseline RPSD and proposed structure showing that while the baseline structure fails at 8µW/mm², the proposed structure stays stable till 300µW/mm².

Spiking band power (SBP) is a neural feature used for motor prediction and is defined as average of absolute signal amplitude in 300-1000Hz [5]. The analog SBP extraction in [4] is compact, but relies on tens of pA of on-current to charge an integration capacitor, which is susceptible to Isc_p. We instead propose an area-efficient and light tolerant digital SBP extraction unit using a flash ADC. It consists of a diode-stack-based VREF generator (12nA, simulation), dynamic comparators with staggered clocks, followed by pulse generators. An asynchronous counter accumulates the total number of fired pulses which integrates the absolute amplitude over the pulse width (Fig. 6, 7). By comparing the counter to a threshold, SBP is symbol-interval-encoded (LED_EN, Fig. 6). LED_EN then fires the LED with a pulse-gap-modulated (PGM) encoding of the mote ID (Fig. 3). Each LED packet consists of a total 17 pulses where the pulse gap (2TCLK/3 TCLK for data 0/1) encodes the 10b unique chip ID (from PUF [6]) and 6b gain configuration (Fig. 10). The LED driver consumes 76nW (simulation) at 50Hz LED firing rate. The ORx allows for data downlink and remote gain control (RGC) (Fig. 9). Two matched 2T-VRs [8] provide DC-bias to the inputs of a hysteretic comparator, AC coupled to VDD and GND. Light modulation toggles the comparator which drives clock and data recovery. The 2T-VRs are size for 1.4nA (simulation) to ensure light robustness, eliminating the light sensitive RSD bias in [4].

Measurments

The proposed IC was fabricated in 180nm CMOS (Fig. 11). In a fully wireless optical setup with an NIR laser for power transfer and downlink and SPAD detector for uplink reception (Fig. 10) the IC can achieve the demandingly low high-pass corner and reduces resistor noise. However, its extremely low conductance, GFB, also makes it susceptible to junction to substrate and deep n-well to p-well photo generated current (Isc_p) (Fig. 4, left). This low conductance vs. Isc_p results in a poor light robustness ratio (RLR = GFB / Isc_p) and the DC-bias level will drift at < 1µW/mm² (simulation). A series-to-parallel switched capacitor-based resistor [7] was proposed to address the process sensitivity of RPSD. However, while it has higher conductance, its hight number of switches results in a large total junction area and high Isc_p and RLR remains poor (Fig. 4, mid). Instead, this work adopts a hybrid approach combining a simple switched capacitor resistor with a 3x attenuator. It maintains a much larger GBR while having a lower Isc_p resulting in a 5·10⁴x improvement in RLR and achieves light tolerance till 350µW/mm² in simulation (Fig. 4, right).

The amplifier achieves 68 dB peak gain, [380, 1060] Hz bandwidth, > 67dB of CMRR and PSRR and, IR of 6.2µVs with 150µW/mm² of incident 850nm LED light at 38°C in measurement which is nearly unchanged from that measured without light (Fig. 5, table). The graph in Fig. 5 plots measured gain across light level for a baseline RPSD and proposed structure showing that while the baseline structure fails at 8µW/mm², the proposed structure stays stable till 300µW/mm².

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References

Fig. 1. Conceptual illustration of NIR based wireless neural recording motes

Fig. 2. Cross section of the CMOS layer with parasitic diode short circuit currents

Fig. 3. Top circuit diagram of the CMOS layer

Fig. 4. Simulated light robustness of three different feedback resistors (top) and proposed light tolerant amplifier (bottom)

Fig. 5. Measured amplifier performance with 850nm light (IR54, CMVision)

Fig. 6. Flash ADC and pulse-counter-based SBP computing unit

Fig. 7. Quantization of absolute amplitude and width from the SBP computing unit

Fig. 8. In vivo measurement setup with RA16PA pre-amp and RX7 Pentasam base station from TTD Inc. (left) and measured waveforms (right)

Fig. 9. ORx structure and operation (top), and measured selective programming waveforms from wireless optical setup (bottom)

Fig. 10. Measured matched filter decoding result (top), and wireless optical setup with NIR laser (QFLD85200S, Qphotonics) and SPAD (SPIFDMNNIR, Aerea) (bottom, left)

Table 1. Comparison Table

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*Measured at 38°C  ** Not Applicable