A Noise-Efficient Neural Recording Amplifier Using Discrete-Time Parametric Amplification

Taekwang Jang, *Member, IEEE*, Jongyup Lim, *Student Member, IEEE*, Kyojin Choo, *Student Member, IEEE*, Samuel Nason, Jeongsup Lee, Sechang Oh, *Student Member, IEEE*, Cynthia Chestek, Dennis Sylvester, *Fellow, IEEE*, and David Blaauw, *Fellow, IEEE*

***Abstract*—This letter proposes an instrumentation amplifier for neural recording applications whose measured noise efficiency factor (NEF) is 2.2. A discrete-time parametric amplifier is adopted as a preamplification stage to lower the input-referred noise, thus improving the NEF. The additional induced sampling noise is minimized by oversampling, and the power overhead for switching is minimized by adopting an 8-phase soft-charging technique.**

***Index Terms*—Instrumentation amplifier, neural recording, noise efficiency factor (NEF), parametric amplifier, soft-charging.**

I. Introduction

Neural recording amplifiers have been widely studied in the last decade to realize small and injectable modules for early detection of brain disorders, such as dystonia, epilepsy, and Parkinson's disease or for restoration of sensory or motor functions. They typically require both aggressive input-referred noise (IRN) and ultralow power consumption to sense the neural potentials accurately while minimizing tissue damage.

Therefore, the noise efficiency factor (NEF), defined as the product of accuracy and power consumption [1], is a key specification of a neural recording amplifier. Even though valuable analog techniques, such as inverter stacking [2] and frequency-domain multichipping [3] have been introduced to approach the ideal NEF of 1 (i.e., NEF of a single bipolar junction transistor), neural recording amplifiers tend to have an NEF larger than 3 because of other stringent specifications. For example, a high common-mode rejection ratio (CMRR) is required to reject electrical interferences. A high power-supply rejection ratio (PSRR) is also important to assure robust monitoring with the presence of supply interferers, such as neighboring channels or the digital back-end circuits sharing the supply voltage. In addition, the minimum frequency of local field potential (LFP) is approximately 1 Hz and is significantly affected by the device flicker noise, while chopping cannot be easily adopted due to the requirement of large input impedance [4]–[6].

In this letter, we propose a neural recording amplifier that achieved an NEF of 2.2 while maintaining the aforementioned specifications [7]. The improvement in noise efficiency is obtained by introducing a discrete-time parametric amplifier as a preamplification stage. The sampling noise of the parametric amplifier is minimized by oversampling, and the power overhead is limited with a stepwise charging and discharging technique [8].

Manuscript received November 27, 2018; revised January 7, 2019; accepted January 28, 2019. Date of publication February 6, 2019; date of current version May 9, 2019. This paper was approved by Associate Editor Alireza Zolfaghari. *(Corresponding author: Taekwang Jang.)*

T. Jang is with the Integrated Systems Laboratory, Swiss Federal Institute of Technology, 8052 Zürich, Switzerland (e-mail: tkjang@iis.ee.ethz.ch).

J. Lim, K. Choo, J. Lee, S. Oh, D. Sylvester, and D. Blaauw are with the Department of Electrical and Computer Engineering, University of Michigan, Ann Arbor, MI 48109 USA.

S. Nason and C. Chestek are with the Department of Biomedical Engineering, University of Michigan, Ann Arbor, MI 48105 USA.

Digital Object Identifier 10.1109/LSSC.2019.2897866

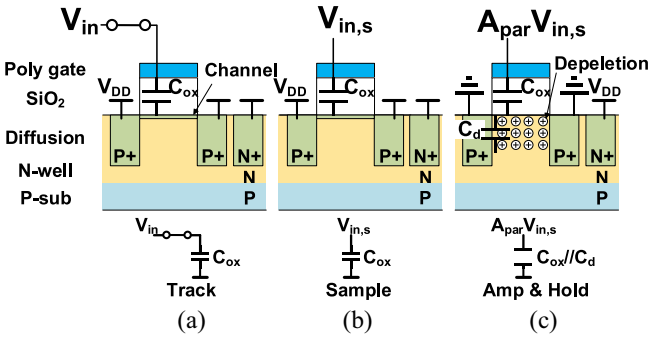

Fig. 1. Cross-sectional view of the pMOS-based parametric amplifier in (a) tracking, (b) sampling, and (c) amplification modes.

II. Operation Principle of Parametric Amplifier

This section briefly discusses the basic operation of a discrete-time parametric amplifier [9] whose gain is obtained by modulating the capacitance of the sampling capacitor. First, during the track phase, the input signal is connected to a pMOS capacitor. The transistor is set to a strong inversion mode so that the oxide capacitance, C_{ox}, is seen at the input [Fig. 1(a)]. Then, a switch disconnects the input and the input voltage is sampled on the capacitor as shown in Fig. 1(b). Finally, the source and drain voltages of the sampling transistor are changed from V_{DD} to the ground [Fig. 1(c)]. As the threshold voltage, $|V_{\mathrm{thp}}|$, of the pMOS transistor increases with higher body-to-source voltage, the transistor is now in a depletion mode. In this case, the sampling capacitance is reduced to a series capacitance of oxide and depletion capacitors $C_{\mathrm{ox}}||C_{\mathrm{dep}}$. As the capacitance is smaller while the total charge on the capacitor is unchanged, the sampled voltage is amplified by the factor of the capacitance ratio

$$A_{\mathrm{par}} = \frac{C_{\mathrm{ox}}}{C_{\mathrm{ox}} \| C_{\mathrm{dep}}}. \tag{1}$$

Fig. 2 shows a simplified schematic of the parametric amplifier and the simulation results. A nonoverlapping clock is provided to track and hold the input signal. A V_{TH} controller toggles the source and drain to either V_{DD} or the ground while both of the switches are open. The simulation results in Fig. 2(b) show a gain of about 4.3.

III. Noise Efficiency

When a conventional amplifier is biased with current I_{tot}, the NEF can be calculated with the following equation [4]:

$$\mathrm{NEF} := v_{\mathrm{rms}} \sqrt{\frac{2 \cdot I_{\mathrm{tot}}}{\pi \cdot U_T \cdot 4kT \cdot f_{\mathrm{bw}}}} \tag{2}$$

where v_{rms}, U_T, k, T, and f_{bw} are the IRN of the amplifier, the thermal voltage, the Boltzmann constant, absolute temperature and the 3-dB bandwidth of the amplifier, respectively. Note that there exists a fundamental tradeoff between the amplifier current and the IRN.

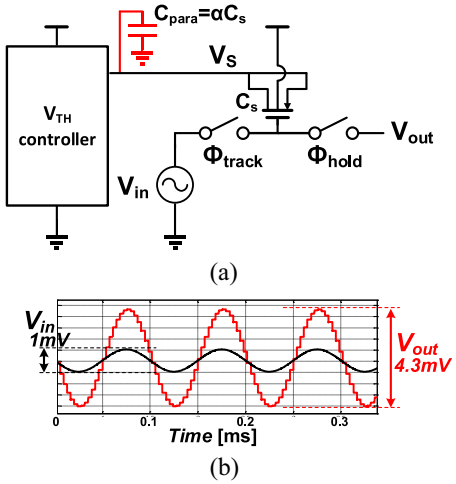

Fig. 2. (a) Simplified schematic of the parametric amplifier. (b) Simulation results.

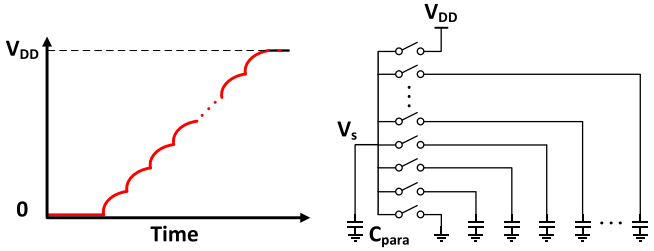

Fig. 3. Operation principle of stepwise charging technique.

Similarly, the NEF of a discrete-time parametric amplifier can be calculated by using the switching current and the sampling noise. The source and drain of the sampling transistor have a parasitic capacitance at their junction to the body. As this parasitic capacitance is proportional to the gate capacitance, it can be expressed as αC_s. Then, the switching current, I_{par}, is $\alpha C_s \cdot V_{\text{DD}} \cdot f_s$, where f_s is the sampling frequency. The sampling noise, kT/C_s, is introduced at the input of the parametric amplifier. Therefore, the NEF of the Nyquist-sampling discrete-time parametric amplifier is

$$\text{NEF}_{\text{par,NS}} = \sqrt{\frac{kT}{C_s}}\sqrt{\frac{2 \cdot \alpha \cdot C_s \cdot V_{\text{DD}} \cdot f_s}{\pi \cdot U_T 4kT \cdot f_s/2}} = \sqrt{\frac{\alpha V_{\text{DD}}}{\pi U_T}}. \tag{3}$$

Assuming α and V_{DD} are 0.25 and 1 V, the NEF of the parametric amplifier is 1.75. However, the small IRN specification of neural recording amplifiers makes it difficult to use the parametric amplifier with Nyquist sampling. For example, if the IRN specification is 3 μV, C_s should be larger than 460 pF, which is impractical to integrate on-chip. Therefore, the input needs to be oversampled so that a small noise level can be achieved using a monolithic capacitor. Assuming a signal bandwidth, f_{bw}, smaller than f_s, and a single-pole located at f_{bw} in the following stage, the IRN is calculated as follows:

$$v_{\text{rms,par,os}} = \sqrt{\frac{kT}{C_s}}\sqrt{\frac{f_{\text{bw}}}{f_s/2}}\sqrt{\frac{\pi}{2}}. \tag{4}$$

Note that $\pi/2$ is multiplied to obtain the equivalent noise bandwidth. Consequently, the NEF of the oversampling parametric amplifier is

$$\text{NEF}_{\text{par,OS}} = \sqrt{\frac{\alpha \cdot V_{\text{DD}}}{2 \cdot U_T}}. \tag{5}$$

We can further improve this NEF by reducing the power for switching the parasitic capacitance by switching V_s adiabatically as proposed in [8]. Instead of switching the parasitic capacitor directly from the ground to V_{DD}, the stepwise charging scheme shown in Fig. 3 changes the voltage by sequentially sharing the charge on the parasitic capacitors with other capacitors defining the intermediate voltages. Note that the intermediate voltages gradually converge to the steady state values after a few iterations of transitions so that they uniformly divide the voltage from ground to V_{DD}. Also the area penalty can be amortized as neural recording front ends are often implemented as an array of large number of channels allowing for the capacitors to be shared. The current is drawn from the supply only at the last step of the transition, reducing the switching current by a factor of the number of steps, N_s. Assuming a uniform voltage distribution, the NEF of the proposed parametric amplifier using stepwise charging scheme is

$$\text{NEF}_{\text{par}} = \text{NEF}_{\text{par,OS}} \Big/ \sqrt{N_s} = \sqrt{\frac{\alpha \cdot V_{\text{DD}}}{2 \cdot U_T \cdot N_s}}. \tag{6}$$

When α, V_{DD}, and N_s are 0.25, 1, and 8, respectively, the NEF of the parametric amplifier is 0.78, which is smaller than the NEF of a single BJT. The NEF can be further improved by increasing N_s with the penalty of additional area for the sharing capacitors.

Because a parametric amplifier can only provide a fixed small gain of A_{par}, it must be followed by a conventional amplifier with a high tunable gain. The NEF of the amplifier chain can be expressed as

$$\text{NEF}_{\text{tot}} = \sqrt{v_{\text{rms,par}}^2 + \frac{v_{\text{rms,amp}}^2}{A_{\text{par}}^2}}\sqrt{\frac{2 \cdot (I_{\text{par}} + I_{\text{amp}})}{\pi \cdot 4kT \cdot U_T f_{\text{bw}}}}. \tag{7}$$

In this paragraph, we will discuss the optimum ratio (β) of I_{par} and I_{amp}. Assuming the NEF of the second amplifier is NEF_{amp}, the IRN of the amplifiers can be expressed as a function of the bias current

$$\begin{aligned} v_{\text{rms,par}} &= \text{NEF}_{\text{par}}\sqrt{\frac{\pi \cdot 4kT \cdot U_T \cdot f_{\text{bw}}}{2 \cdot I_{\text{par}}}} \\ v_{\text{rms,amp}} &= \text{NEF}_{\text{amp}}\sqrt{\frac{\pi \cdot 4kT \cdot U_T \cdot f_{\text{bw}}}{2 \cdot \beta \cdot I_{\text{par}}}}. \end{aligned} \tag{8}$$

Rewriting (7) using (8) gives us the following equation:

$$\text{NEF}_{\text{tot}}^2 = (1+\beta)\left(\text{NEF}_{\text{par}}^2 + \frac{\text{NEF}_{\text{amp}}^2}{A_{\text{par}}^2 \cdot \beta}\right). \tag{9}$$

The optimal β can be found by equalizing the derivative of (9) to 0

$$\beta_{\text{opt}} = \frac{1}{\alpha C_s V_{\text{DD}}}\frac{I_{\text{amp}}}{f_s} = \frac{\text{NEF}_{\text{amp}}}{A_{\text{par}} \cdot \text{NEF}_{\text{par}}}. \tag{10}$$

Consequently, the optimum total NEF is

$$\text{NEF}_{\text{tot,opt}} = \text{NEF}_{\text{par}} + \frac{\text{NEF}_{\text{amp}}}{A_{\text{par}}}. \tag{11}$$

It can be seen that the total NEF improves compared to NEF_{amp} if NEF_{amp} is larger than $\text{NEF}_{\text{par}} \cdot A_{\text{par}}/(A_{\text{par}} - 1)$, which is 1.016 when NEF_{par} and A_{par} are 0.78 and 4.3, respectively. Therefore, the proposed parametric amplifier technique is useful for neural recording applications whose NEF is typically higher than 3.

IV. Proposed Amplifier Design

Fig. 4 shows the overall schematic of the proposed neural recording amplifier chain. Two parametric amplifiers are interleaved so that the clocks are shared while doubling the sampling frequency (Fig. 5). The transition on V_s node is divided into eight phases, effectively lowering the switching power by the same factor.

The following amplifier chain is composed of two stages: 1) a low-noise amplifier (LNA) and 2) a variable gain amplifier (VGA). The VGA is designed in a fully differential operational transimpedance amplifier (OTA) structure using an inverter-based input stage to minimize its IRN. The gain of VGA is determined by the capacitance ratio of input and the feedback capacitors.

The parametric amplifier gain is determined by the pMOS capacitance ratio. Therefore, it is important to minimize the input

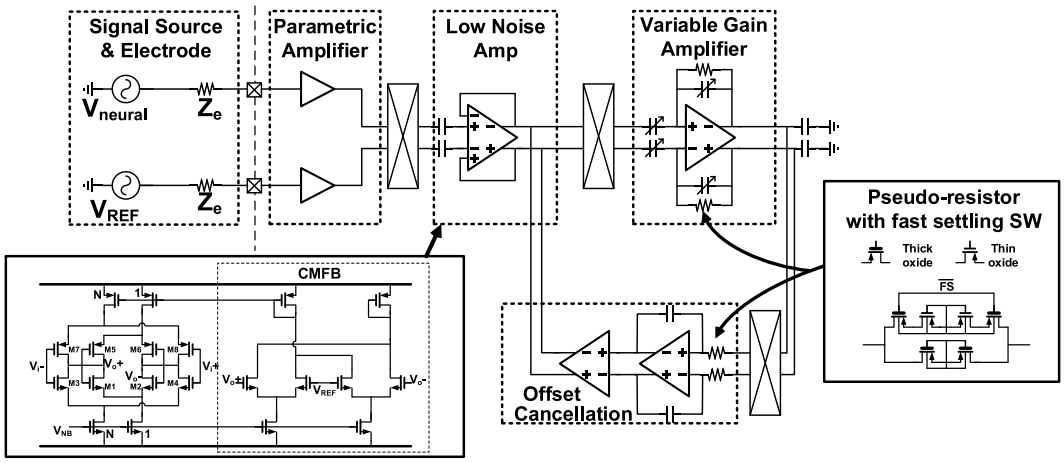

Fig. 4. Overall schematic of the proposed instrumentation amplifier for neural recording.

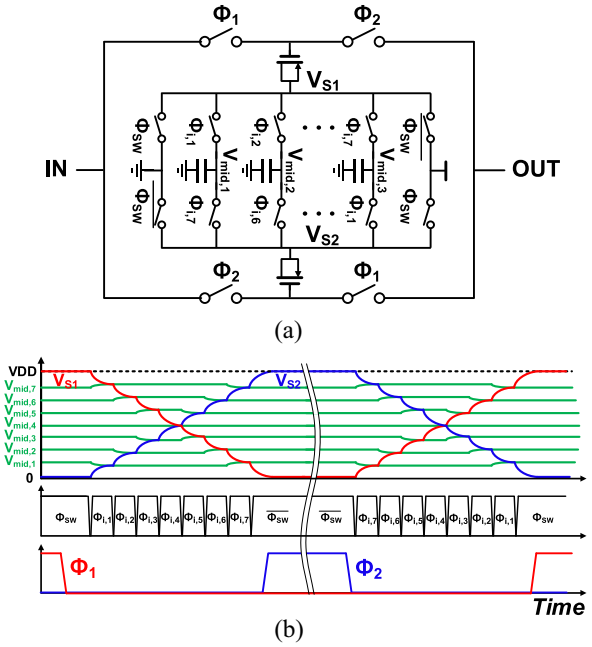

Fig. 5. (a) Schematic and (b) waveforms of the proposed discrete-time parametric amplifier with 8-phase soft-charging technique.

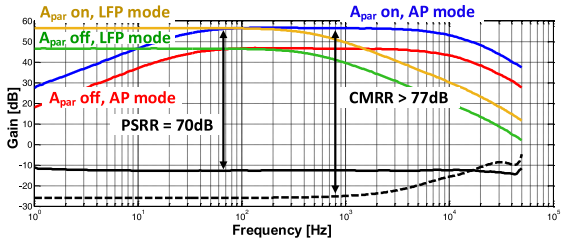

Fig. 6. Measured transfer function of the proposed amplifier plotted with its CMRR and PSRR.

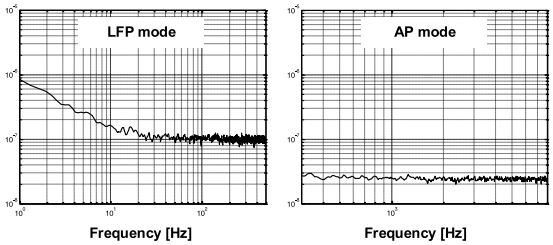

Fig. 7. Measured IRN spectral density.

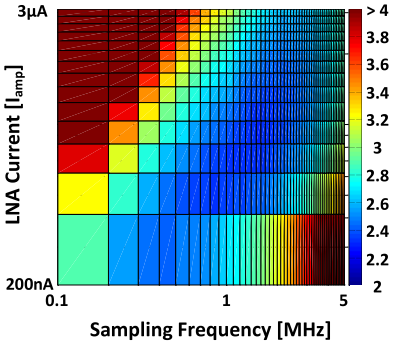

Fig. 8. Measured NEF while varying the sampling frequency and LNA bias current.

capacitance of the LNA to maximize the parametric amplifier gain. However, the conventional differential amplifier, whose gain is defined by the input and feedback capacitors, has a relatively large input capacitance connected to its virtual ground. In this letter, we adopted an LNA stage whose gain is defined by the ratio of transconductance, g_m. As g_m is proportional to the bias current when the transistors are operating at a subthreshold region, the gain can be accurately controlled using the bias current ratio. An inverter-based input stage is adopted to minimize the NEF by maximizing input g_m.

To achieve high resistance for a low cut-off frequency less than 1 Hz for LFP recording, we used IO devices to form a pseudo-resistor and have the unity-gain feedback of OTAs. The settling time was improved by a fast settling switch with a low impedance path.

The chopping of LNA is implemented to reduce the flicker noise during LFP recording. The ripple induced by the input offset of LNA is suppressed through the offset cancelation amplifier, which is composed of a differential integrator and an OTA. Typically, the chopping results in reduced input impedance, which is highly disadvantageous in neural recording applications where the source impedance can exceed 1 MΩ. The LNA of the proposed amplifier, on the other hand, can achieve much smaller input capacitance by designing the amplifier with smaller devices because its input-referred flicker and thermal noise are attenuated by A_{par}.

V. Measurement

The proposed amplifier was fabricated in 0.18-μm CMOS technology. Fig. 6 illustrates the gain of the proposed amplifier in both AP

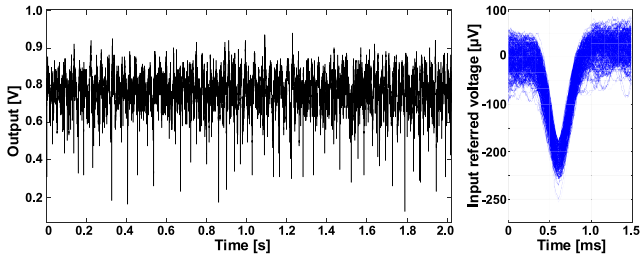

Fig. 9. Transient measurement results using previously recorded data (*in-vivo*) and the time-aligned spikes.

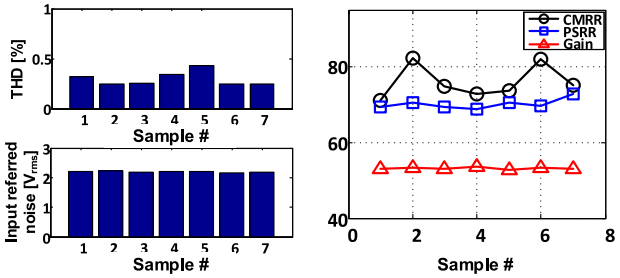

Fig. 10. Schematic of the proposed discrete-time parametric amplifier with 8-phase soft-charging technique.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON

	This work		[4]	[5]	[6]
Power (μW)	5.5		2.8	2.8	7.02
Input referred Noise (μV_{rms})	AP: 2.3 LFP: 3.4		4.13	AP: 5.2 LFP: 1.8	AP: 3.2 LFP: 5.8
Bandwidth (Hz)	1-8000		1-8200	1-5000	0.5-6000
NEF	Parametric Amp	0.85	2.93	AP: 4.4 LFP: 7.4	AP: 3.08
	Total Amp. front-end	AP: 2.2 LFP: 3.1			
Gain (dB)	30-60		57.8	25.7	30-72
Signal type	AP+LFP		AP+LFP	AP+LFP	AP+LFP
Input common mode range (mV_{pp})	100		200	40	-
Input impedance (MΩ)	147		-	1600	-
PSRR (dB)	> 70		78	-	70
CMRR (dB)	> 70		> 80	-	60
THD	1% ($5mV_{pp}$)		-	-76 dB	1% ($18mV_{pp}$)
Size (mm^2)	0.071		0.042	0.069	0.088[1]
Technology	0.18μm		65nm	65nm	0.18μm

and LFP measurement modes. The gain difference is around 10 dB (A_{par}) when an identical VGA setting is used. The measured PSRR and the CMRR are all larger than 70 dB.

The IRN spectral densities are plotted in Fig. 7. The measured IRN of the LFP and AP modes are 3.4 and 2.3 μV, respectively. The amplifier chain is configured to consume lower power in LFP mode (0.38 μW) because lowering the thermal noise floor is not efficient due to the smaller bandwidth and VGA flicker noise. The noise floors are 100 and 24.5 nV/$\sqrt{\text{Hz}}$ in LFP and AP modes, respectively.

The NEF of the proposed amplifier is measured while sweeping the sampling frequency of the parametric amplifier and the bias current of LNA (Fig. 8). As an example, the top left corner is a case where the LNA current is overused because the noise is dominated by the sampling noise of the parametric amplifier. Whereas, the bottom right corner is when the switching power is wasted while the noise is dominated by the following LNA. As discussed in (10), there exists an optimal ratio between the sampling frequency and the amplifier bias current, as noted by blue region shown in Fig. 8. Fig. 9 shows the recorded data and time-aligned spikes in AP mode.

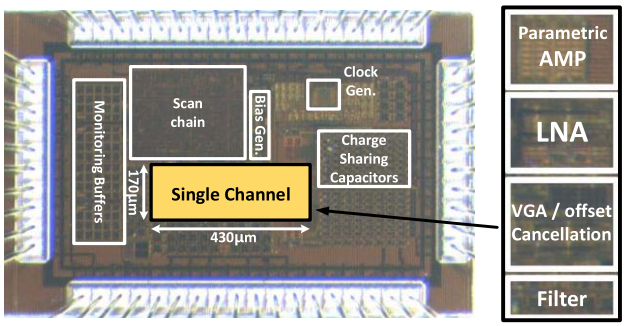

Fig. 11. Die photography.

The design was tested with seven samples, as shown in Fig. 10. The total harmonic distortion is measured less than 0.5% with 2-mV peak-to-peak input. The measured IRN varies from 2.15 to 2.2 μV. Both the measured CMRR and PSRR are higher than 70 dB, and the gain variation is less than 1.2%.

Table I summarizes the performance of the proposed amplifier compared with state-of-the-art designs. The NEF in AP and LFP modes are 2.2 and 3.1, respectively, The input common mode range is 100 mV, and the measured input impedance is 147 MOhm when chopping is enabled. An amplifier chain for a single channel occupies 170×430 μm^2, as shown in Fig. 11.

VI. CONCLUSION

In this letter, a discrete-time parametric amplifier using an 8-phase soft-charging scheme is introduced. The noise and power analysis of the parametric amplifier is discussed. The proposed scheme potentially offers a chance to achieve lower than 1 NEF with a larger number of intermediate phases. By using the parametric amplifier as a preamplifier, 2.2 NEF was achieved while showing excellent immunity to environmental interferences.

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