Enabling Closed-Loop Neural Interface: A Bi-Directional Interface Circuit with Stimulation Artifact Cancellation and Cross-Channel CM Noise Suppression

Adam E. Mendrela, Jihyun Cho, Jeffrey A. Fredenburg, Cynthia A. Chestek, Michael P. Flynn, and Euisik Yoon

University of Michigan, Ann Arbor, MI,

Abstract

We present the first bi-directional neural interface chip that employs a stimulation artifact cancellation circuit to allow concurrent recording and stimulation. In order to further suppress cross-channel common-mode noise, we incorporated a novel common average referencing (CAR) circuit in conjunction with range-adapting (RA) SAR ADC for low-power implementation. The fabricated prototype attenuates stimulation artifacts by up to 42 dB and suppresses common noise among channels by up to 39.8 dB at 330 nW and in an area of 0.17 mm^2 per channel.

Introduction

Implanted neural interface microsystems promise treatments for neurological disorders such as epilepsy and spinal cord injuries through closed-loop control of neural stimulation [1]. Such applications require continuous monitoring during the onset of stimulation, often rendered impossible due to large, channel-saturating artifact. Few systems attempt to mitigate this problem by blanking the recording channel during stimulation or with self-cancelling stimulation electrode configuration [2]. These solutions, however, are limited by reduced sensing capability and electrode array design. Additional noise sources from power-line and motion artifacts also prevent practical deployment in target clinical settings and have not yet been fully addressed in microsystem architectures. In this paper, we present a neural interface system that incorporates three novel techniques to address these challenges while maintaining low power: (1) a stimulation artifact cancellation filter to prevent recording channel saturation, (2) an analog-domain common-average referencing (CAR) circuit to suppress cross-channel common-mode noise, and (3) a range-adapting (RA) SAR ADC that utilizes neural signal sparsity to reduce power consumption.

System Architecture

Our prototype neural interface design, (Fig. 1), has 8 recording and 4 stimulation channels. Each recording channel consists of a capacitively-coupled 40dB gain preamplifier with bandwidth (BW) control, a CAR network, a programmable-gain amplifier (PGA) with BW and gain control, and a 10 bit RA SAR ADC. Analog blocks use 1V supply voltage while digital blocks use 0.5V supply The nominal recording bandwidth is from 0.1 Hz to 2 kHz, and can be adjusted for different types of neural signals (such as for ECoG or EEG). The stimulation module can supply configurable current pulses of up to 8 mA. A stimulation artifact cancellation filter (StimC Filter) learns the stimulation artifact waveforms by correlating the recorded signal with the stimulating signal. The filter then subtracts the artifact in the preamplifier on the fly.

A. Stimulation Artifact Cancellation Circuit

We introduce a new adaptive-filter-based technique to remove stimulation artifacts during recording without compromising the recording quality. The new approach is inspired by crosstalk cancellation in wireline communication. By correlating the stimulation signal with the artifacts in the recorded signal, a digital filter learns the transfer function from the stimulator to the input and then subtracts the artifacts from the input of the preamplifier. Equations and conceptual diagram in Fig. 2 describe this simplified least mean squares (LMS) algorithm. To substantially reduce the LMS filter complexity and power consumption, only the sign bit of ADC output (E(t)) and stimulation signal (u(t)) are processed by the filter. This digital filter is implemented with eight 8-bit taps with 1 bit inputs, 8 ripple-carry adders, 72 flip flops, and AND gate 1-bit multipliers. The output of the filter ($\hat{y}(t)$) drives the cancellation 8-bit differential capacitor DACs connected at the inputs of the preamplifier. The scheme reduces 8-sample long artifacts by up to 42 dB.

B. Common-Average Referencing (CAR) Circuit

We also introduce a novel front-end circuit-based Common Mode noise rejection technique known as CAR. CAR is increasingly used in neuroscientific experiments but as a software post-processing algorithm [3]. In many neural recording systems, neural tissue noise couples more strongly to the input channels than to the shared low-impedance reference node. Because the noise coupled to the reference electrode is far weaker than at the recording electrodes, the overall noise cannot be rejected by the CMRR of the amplifiers. Instead, by spatially averaging multiple channels, we create a *common average* reference signal and subtract it from each channel to remove common noise before it saturates the PGA or the ADC. We implement CAR by connecting every preamp output to each PGA input within every 4-channel group through a capacitive averaging circuit (Fig. 3). The user can select channels to be referenced and adjust the gain with switch programmable caps, C_{in} and C_{FB}. The CAR circuit reduces common noise by up to a measured ~40 dB.

C. Range-Adapting (RA) ADC

A new RA SAR ADC facilitates low-power operation. Our scheme works well in neural recording where the neural signals are close to 0V (i.e. code 512) for most of the time. As the ADC adjusts its dynamic range between samples, an on-chip FSM periodically decrements the range during times of little activity to save SAR cycles and increments the range when the ADC observes a larger signal (Fig. 4(a)). RA SAR algorithm, (Fig. 4(b)), begins the SAR search at the previous sample magnitude, checks whether the sample is in range or if the range should be increased, and then completes the SAR search from the new MSB with the efficient merged capacitor switching (MCS) method. Fig 4(c,d) show the reduction in the number of SAR cycles and the associated total switching energy per code as compared to a conventional full range (FR) MCS ADC. For neural signals dominated by moderate amplitude activity, our scheme is more efficient than [4] which always begins the SAR search at the LSB. For a typical neural signal sequence, the ADC saves approximately 10% of SAR cycles and 47% of DAC switching energy compared to FR conversion.

Measurements

The prototype is fabricated in 0.18um CMOS and occupies

1.58 mm^2. The recording channels consume an average of 2.64 µW (330 nW per ch.) for a 1 Hz – 2 kHz amplifier bandwidth and a sampling rate of 4 kS/s. Fig. 5(a) shows the channel gain vs. frequency plot for 4 different gain settings (1, 2, 5, and 10). The input-referred noise is 3.05 μV_{rms} (Fig. 5(b)). Fig. 6 shows the measured DAC energy consumption of RA ADC at low input voltages in comparison with full range SAR ADC. Our measurements also show a low DNL between +/-0.3 LSB. In Fig. 7(a), the stimulation artifact cancellation circuit successfully learns and removes artifacts from the recorded channel when stimulation is activated for a nearby ECoG probe in an *in-vitro* experiment in an agar-based phantom and with epilepsy-induced rat data. Another experiment showed a 26.5 dB reduction of 60 Hz noise with CAR (Fig. 7(b)). Fig. 8 shows the die microphotograph. A summary table (Fig. 9) shows that our work achieves state-of-the-art performance with NEF (Preamp+PGA+ADC) of 1.63 while including novel features that enable the use in clinical applications.

References

[1] W. Chen et al., *ISSCC*, 2013 [2] S. Stanslaski et al., *TNSRE*, 2012
[3] K. Ludwig et al., *Journal of Neurophysiology*, 2009
[4] F. Yaul and A. Chandrakasan, *ISSCC*, 2014
[5] F. Zhang et al., *JSSC*, 2013 [6] R. Muller et al., *ISSCC*, 2014

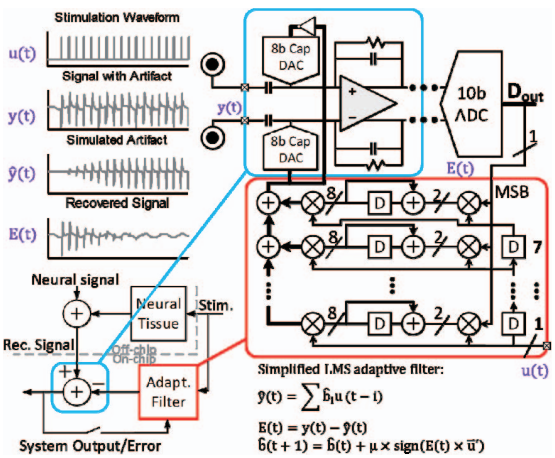

Fig. 2 Conceptual diagram and schematic of stimulation artifact cancellation

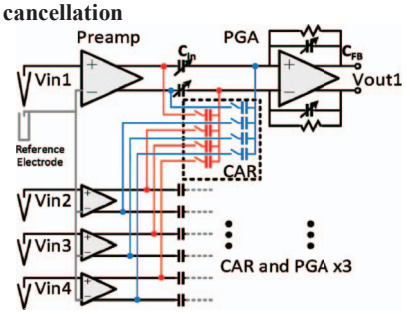

Fig. 3 Common average referencing (CAR) – PGA schematic

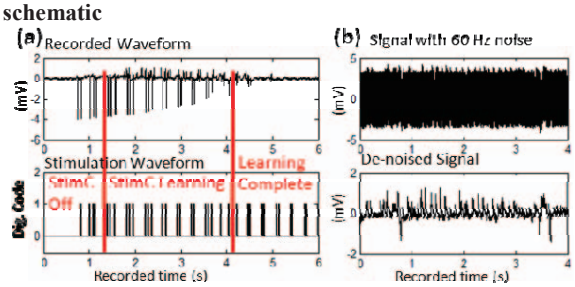

Fig. 7 (a) Stimulation artifact cancellation and (b) CAR 60 Hz de-noising example in *in-vitro* recordings

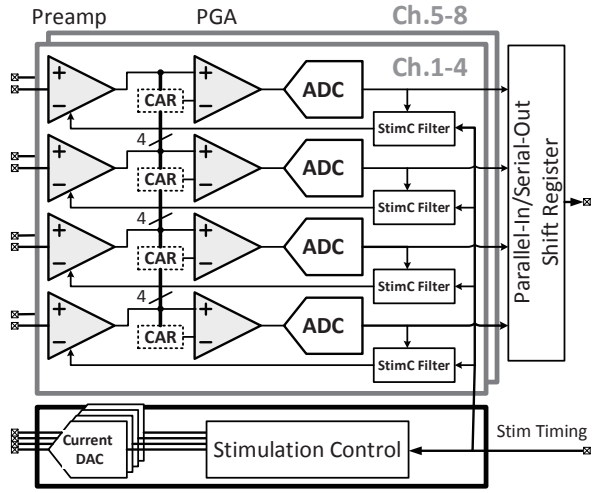

Fig. 1 Top-level system architecture diagram

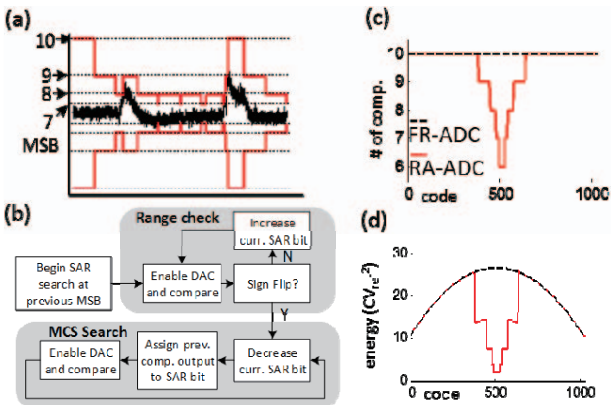

Fig. 4 (a) ADC range adapting to neural signal, (b) RA SAR ADC logic flow, (c) minimum number of SAR cycles and (d) minimum DAC energy per code

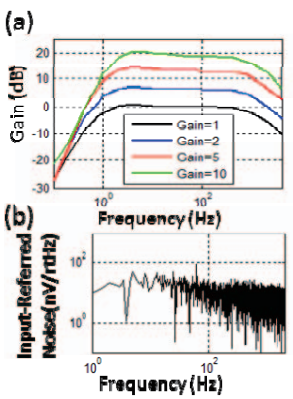

Fig. 5 (a) Analog gain vs. frequency and (b) input-ref. noise (with ADC)

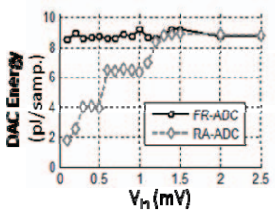

Fig. 6 DAC energy consumption comparison

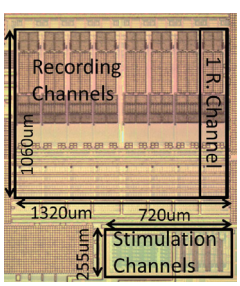

Fig. 8 Die micrograph

	[1]	[5]	[6]	This Work
Technology	0.18 µm	0.13 µm	65 nm	0.18 µm
Area (per rec. ch.) (mm²)	~0.42	~0.625	0.025	0.17
Rec. Power (µW/ch.)	7.35	4.2	2.3	0.33
BW (~Hz)	~0.5 – 7k	0-320	1 – 0.5k	1 – 2k
IR Noise (μV_{rms})	5.23	2	1.43	3.05
Stim. Artifact Cancellation	N	N	N	Y
CAR	N	N	N	Y

Fig. 9 Summary and comparison chart