Neurodynamic Interface Circuits for a Multichannel, Wireless Sensor IC Operating in Saltwater

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Abstract- This paper presents the amplifier and stimulator circuits, as well as 50-Ω antenna driver, that augment a multichannel, wireless sensor interface platform IC for use in neurodynamic studies of a sea animal, *Aplysia Californica*. The prototype chip, including the platform and 2-channel neurodynamic interface circuits, has been fabricated in a 0.5-µm CMOS process, occupies an active area of just 0.7 mm^2 and consumes 3.56 mW. This would allow 120 hours of recording using 160mAh lithium ion battery. Test results of the interface circuits are presented and exhibit the desired performance.

I. Introduction

Low-power and robust, wireless microsensors are required for applications requiring unobtrusive sensing in harsh operating conditions, e.g. high-temperature and mechanically/chemically active environments. Such conditions are common to applications such as automotive and aerospace engine control; and in-vivo bio-sensing. In previous work [1], platform circuits were developed to support such applications.

In this work, custom integrated circuits were developed to enable untethered neurodynamic studies of a common sea slug, *Aplysia Californica*. These prototype circuits, specifically a low-noise neural amplifier, a programmable neural stimulator, and an efficient, 50-Ω/1-mW antenna driver were combined with the platform circuits to enable a low-power, single-chip system that can be surgically implanted in this saltwater animal and used to monitor and stimulate neural activity.

II. Platform Circuits

A. Overview

A general platform for wireless sensing in harsh environments, including a sigma-delta (Σ-Δ) analog-to-digital converter (ADC), frequency shift keying (FSK) modulator, linear voltage regulator, on-chip oscillator and clock generator, is shown in Figure 1. This platform circuitry was first described in [1], and is briefly reviewed here.

B. Sigma-Delta Analog-to-Digital Converter

An oversampling switched-capacitor (SC) 1st-order Σ-Δ ADC is designed to convert the amplified neural signal to 1-bit digital stream. Dither is added to disturb the limited cycle oscillation problem occurring at the low-amplitude input to improve the modulator resolution. Chopper stabilization and dynamic element matching are used to minimize the effect of imperfect circuit components.

A decimation filter is included to remove the out-of-band noise in the Σ-Δ ADC output and reduce the bit rate. A parallel-to-serial converter was incorporated to convert the parallel decimator output to serial bit stream, and is combined with the channel information and the header information.

C. FSK Modulator

As shown in Figure 1, an inductor and a capacitor are required to make the FSK modulator oscillates at the desired transmit frequency. The fundamental frequency f_0 is given by

$$f_0 = \frac{1}{2\pi\sqrt{LC}}. \quad (1)$$

Taking the derivative of (1) with respect to C yields

$$\Delta f \approx \frac{f_0}{2}\left(\frac{\Delta C}{C}\right) \quad (2)$$

In this work, the 27-MHz ISM band is used. Given an inductance of 200 nH, the nominal tuning capacitance is 173 pF, so $\Delta f / \Delta C = 80 kHz / pF$. To support a bit rate of 80 kbps with a relatively simple receiver design, the frequency deviation Δf should be 160 kHz, so ΔC has been set to 2 pF. MOS switches controlled by the input digital signal are used to switch ΔC in an out of the circuit to shift the oscillation frequency. An off-chip variable resistor is used to adjust the bias current to optimize the trade-off between negative conductance and power consumption, although this off-chip component could ultimately be eliminated.

D. Oscillator and Clock Generator

Absolute accuracy of the clock generator is not essential for this work, but the clock period has to be sufficient to allow the switched-capacitor (s-c) circuitry in the ADC to settle accurately. The platform circuits include a fully-integrated oscillator to provide the clock, based on a three-stage differential ring whose frequency is locked to the settling time of the fully-differential operational amplifier (FDOA) used in the ADC. The oscillator provides a nominal clock frequency of 1MHz.

III. Circuits for Wireless Neurodynamic Studies

A. Neural Amplifier

This section discusses the amplifier that has been designed for recording action potentials from nerve cells. The schematic of the neural amplifier, modeled after [2] is shown in

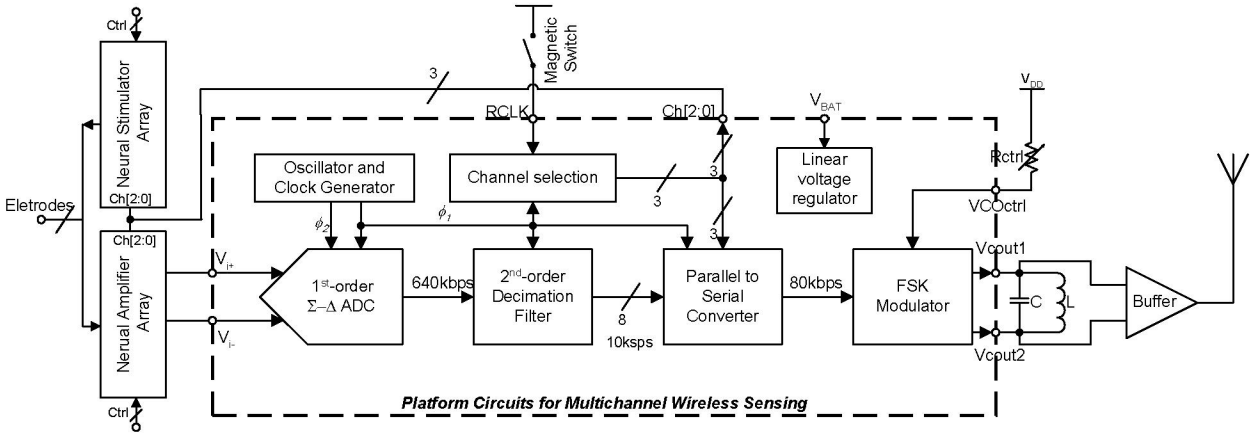

Figure 1. Block diagram of the wireless sensor interface integrated circuit for neurodynamic studies.

Figure 2. The capacitive input blocks the large dc drift that is common in biological recording, especially in the saltwater environment. The ratio $C_1/C_2 = 100$ sets the passband gain. The low-frequency cutoff is set by the parallel combination of the feedback capacitor and the small-signal resistance of M1-M2, which can be very large, exceeding 10^{12} Ω. Thus a low-frequency cutoff below 1 Hz is possible using very little die area for the passive devices. The high-frequency cutoff of this bandpass amplifier is determined by amplifier g_m and load capacitance. In this prototype, no specific load capacitance has been included, so bandwidth is limited only by the analog buffer used to drive the off-chip load capacitance.

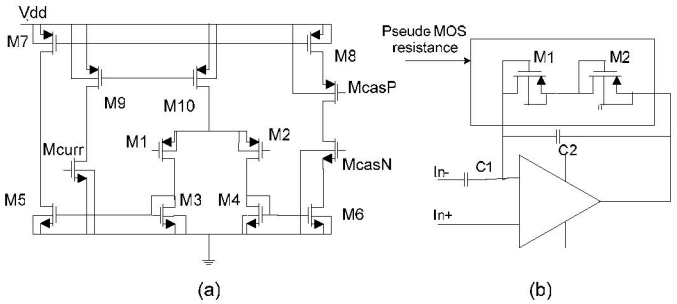

Figure 2. Circuit schematic of the neural, bandpass amplifier (after [2]).

Low-power is desirable for multichannel operation. This design uses a 2.7V power supply to lower power consumption; but this limits voltage swing. The design is optimized to achieve maximal voltage swing while maintaining low-noise operation. The trade-off here is: low V_{DSAT} is required for higher swing but this increases g_m, thereby increasing thermal noise. The maximum output voltage is determined by the sum of V_{DSAT} of M8 and McasP and the minimum output voltage by the sum of V_{DSAT} of M6 and McasN. The V_{DSAT} was distributed optimally between M8 and McasP. M8 has higher V_{DSAT} so that its thermal noise contribution is low, while, V_{DSAT} of McasP was kept low. This would increase thermal noise of transistor McasP, but its contribution to the total input referred noise will be less due to two stage gain. Thus, this design achieves lower noise for optimum voltage swing.

Wide transistors are used in the input differential pair to reduce flicker noise. This also decreases overall input referred thermal noise [2]. These transistors are biased in sub-threshold region, which results in low power operation. The tail current is designed to be 10uA.

A. Neural Stimulator

The neural stimulator consists of an adjustable current source and corresponding digital control lines, as shown in Figure 3. A current of amplitude +/- 50 to 400 uA is required through a load resistance of ~5 kΩ for pulses lasting several milliseconds. A reference current, I_{Ref}, is created using an external resistor and an NMOS transistor. This current is mirrored to create three NMOS and three PMOS complementary current sources, with amplitudes 1x, 2x, and 4x I_{Ref}. Amplitude control logic, Ictl2:0, selectively connects these sources to the output using NMOS and PMOS switches (110 Ω and 370 Ω respectively) for an output range of 0x to 7x I_{Ref}. A polarity control signal, pos, connects the positive or negative current to *a* or *b* output. Finally, transmission gate switches (110 Ω) disconnect the amplifier circuitry whenever stimulation is enabled using the stim signal.

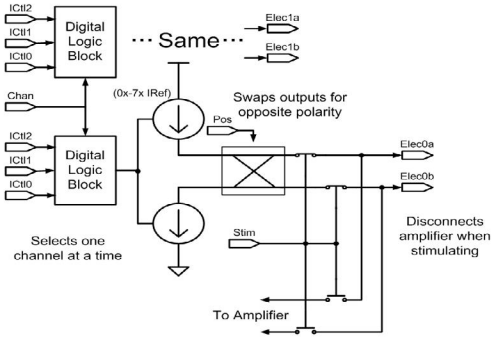

Figure 3. Block diagram of the neural stimulator.

B. Antenna Driver and Matching Circuit

In [3], an electric dipole antenna that provides 50-Ω impedance in the saltwater environment of these neurodynamic studies was described. In this work, an efficient antenna driver and matching circuit has been proposed for use with this 50-Ω

antenna, using minimal on-chip and off-chip components, as illustrated in Figure 4. The complementary FSK signal produced by the FSK modulator is supplied to inputs *d* and *dB*. These inputs are buffered and driven by simple inverters formed by CMOS transistors M1a/b and M2a/b. The inverter outputs are coupled to the differential outputs of the IC through double-poly capacitors C1a/b, which are set to 250 fF. The on-chip capacitors form capacitive voltage dividers with external capacitors Ca/b that provide an efficient attenuation of the 2.7-V supply voltage. The result is $V_{a,b}$ = 245-mV singled-ended square waves that are driven through equivalent capacitances of 2.75 pF. The rms value of the first harmonic of the differential square wave is $(2\sqrt{2}/\pi)\ V_{a,b}$ = 220 mVrms, which provides 1 mW of power into 50 Ω.

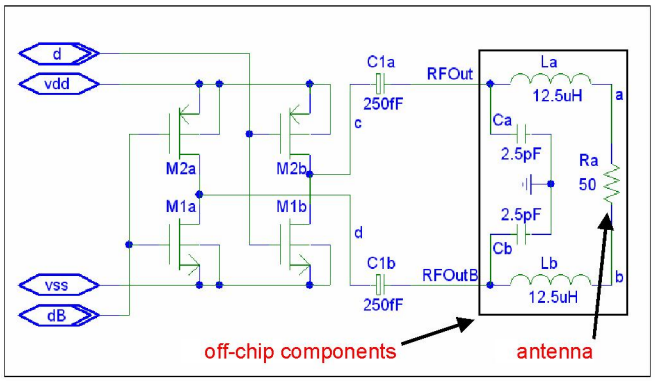

Figure 4. Circuit schematic of the antenna driver circuit with off-chip matching network.

The matching circuit consists of parasitic capacitors Ca/b, adjustable inductors La/b, and the 50-ohm antenna. Capacitors Ca/b are "free" and include bonding pad, package, and PCB capacitance. Inductors La/b are implemented using adjustable cylinders and will be tuned to the desired transmission frequency of 27 MHz. Their nominal values are calculated to provide a 320-kHz bandwidth when connected in series with the 50-ohm antenna resistance.

Inverters are implemented using minimum channel lengths (0.6 μm) and a pmos:nmos width ratio of 3:1 to obtain symmetric on resistance. SPICE simulations were performed to find the device widths that balance the trade-off between CV^2f power loss due to capacitance at the outputs of the inverters, and I^2R_{on} loss due to the relatively high current being driven into the 50-Ω antenna. Minimum power loss occurred when transistors widths were set to 72/24 μm for PMOS/NMOS, and power efficiency is 80%, i.e. 1.07 mW is provided by the supply and 0.86 mW of fundamental power is delivered to the antenna.

IV. Test Results

A prototype chip including the wireless platform and two channels of neurodynamic circuitry with antenna driver was fabricated in the AMI 0.5-μm n-well CMOS process. The die microphotograph is shown in Figure 5. The active circuits occupy an area of 0.7 mm^2.

Figure 6 shows the measured frequency response of the neural amplifier. The gain is ~ 40dB (90) and low pass cut-off frequency is 105 kHz. Voltage gain is slightly lower than 100 because of finite open loop gain of the neural amplifier. The low pass cut-off is higher than the ultimate goal since the output of the neural amplifier has not been loaded with a band-limiting capacitor in this prototype. The high pass cut-off frequency cannot be examined in this test since it is below the range of our measurement equipment.

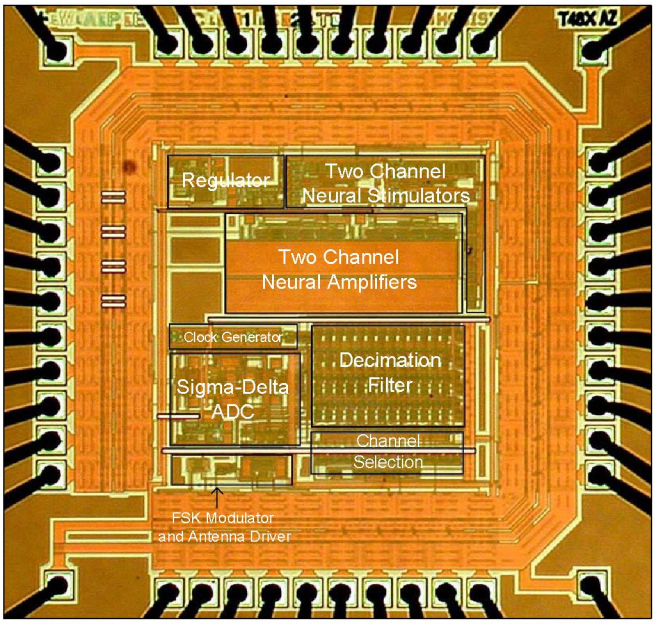

Figure 5. Die microphotograph.

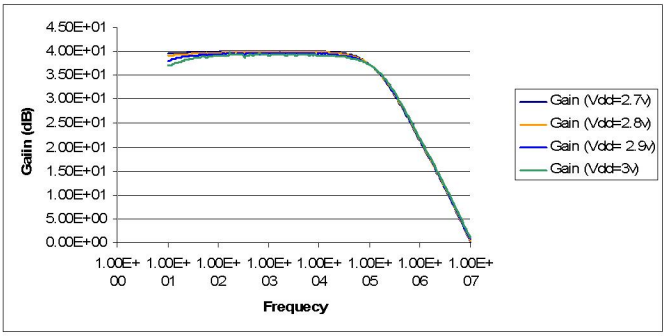

Figure 6. Measured frequency response of the neural amplifier. The 3-dB bandwidth has not been limited by a load capacitor in this prototype.

Figure 7 shows the measured step response of the neural amplifier. The high pass cut-off frequency corresponding to the fitted transient response is 0.7 mHz. Figure 8 shows the measured output noise spectral density of the amplifier, from which the input referred noise of the amplifier is determined to be 4.27 μV rms over a 10 kHz bandwidth.

As shown in, the neural stimulator has measured nonlinearity less than 8 μA (1% full scale) in nominal operation conditions with a reference current of 57 μA and load of 5 kΩ. The output resistance is between 50 and 500 kΩ depending on the

number of sources enabled. The output current was measured using a variety of load resistors, and the result is shown in Figure 10. The measured rise/fall time of the output current is ~1 µs, which is easily fast enough for the neuron stimulation rates of 80 Hz.

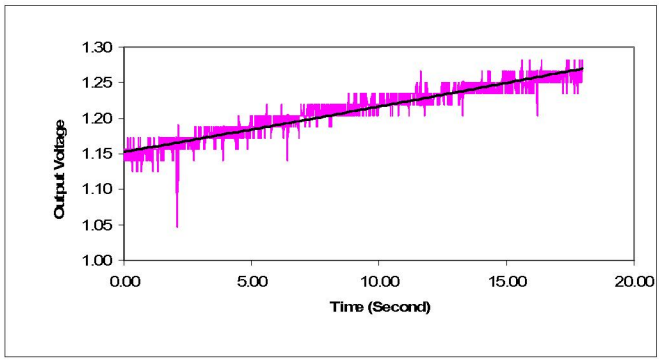

Figure 7. Measured step response of the neural amplifier. The smooth line is a 1st-order exponential decay that has been fit to the measured response.

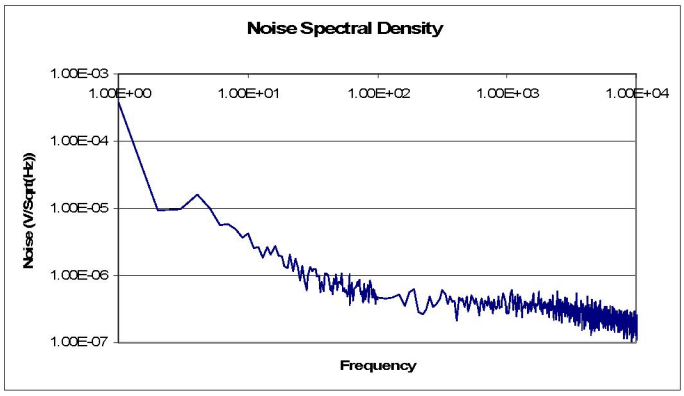

Figure 8. Measured input-referred noise spectral density

The antenna driver circuit has been tested for functionality but work continues to optimize the off-chip portion of the matching circuit to obtain precise results on transmitted power and power efficiency.

Table 1 shows measured or estimated power consumed by various sections of the IC. The total power consumed by the IC (excluding analog buffer for testing) is 3.56 mW. This would allow 120 hours of recording using 160mAh lithium ion battery.

Table 1. Power consumed by various sections of the IC

** Power for antenna driver depends on the off-chip matching circuit, which is a work in progress*

Section of IC	Power (mW)
Regulator + bias	0.19 (Measured)
FSK Modulator	0.08 (Estimated)
Antenna driver	2.00* (Estimated)
2*Amplifier +Oscillator+ADC	1.29 (Calculated)
Complete Test IC – Analog Buffer	**3.56 (Calculated)**
Analog Buffer	5.4 (Estimated)
Complete Test IC	8.96 (Calculated)

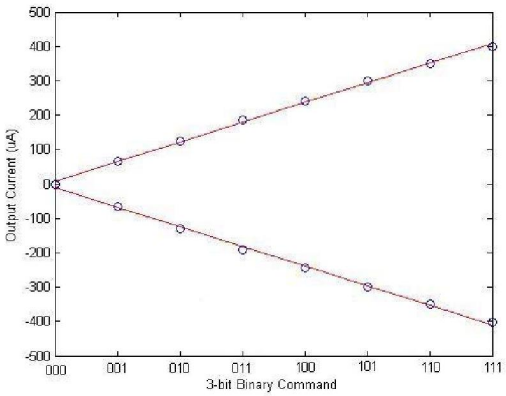

Figure 9. Measured response of the neural stimulator.

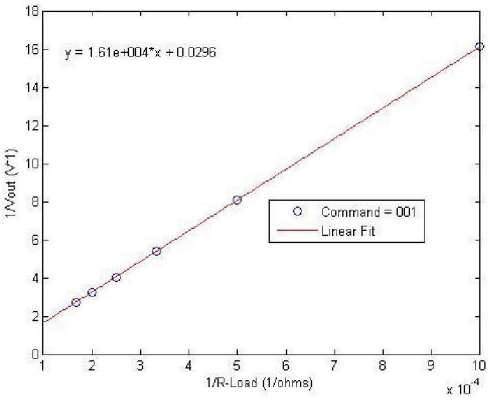

Figure 10. Measured effect of load resistance on the output current of the neural stimulator. The fitted line indicates an output resistance of 59 kΩ.

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